TCU 09 memory map (17th March 2010)

Overview

| *Memory Block* | *Starting Address* | *Ending Address* | *Number of Addresses* | *Data Mask* |
|---|---|---|---|---|
| Mother CSRs | 0x YY00 0000 | 0x YY00 00FC | 64 | Various |
| Daughter CSRs | 0x YY00 0100 | 0x YY00 0FFC | 960 | Various |
| Trigger Registers | 0x YY10 0000 | 0x YY1F FFFC | 2^18 (256K) | Various |
| Counter Registers | 0x YY20 0000 | 0x YY2F FFFC | 2^18 (256K) | Various |
| Input Memory | 0x YY40 0000 | 0x YY5F FFFC | 2^19 (512K) | 0x FFFF FFFF |
| Output Memory | 0x YY60 0000 | 0x YY7F FFFC | 2^19 (512K) | 0x FFFF FFFF |

Mother CSRs

| *ID: Name* | *Address* | *Functionality (default)* | *Access* |
|---|---|---|---|
| 0:Mother firmware rev | 0x YY00 0000 | 0xABCDmmmm | R |
| 1:Status | 0x YY00 0004 | D0: RCC_halt<br>D1: RCC_latch<br>D2: RCC_run_stop<br>(these default to '1' when unconnected) | R |
| 2:Halt status/control | 0x YY00 0008 | TBD | |
| 3:RCC/Local clock mode | 0x YY00 000C | D0: 0=RCC, 1=Local | RW |
| 4:Local mode run/stop | 0x YY00 0010 | D0: 0=Stop, 1=Run | RW |
| 5:Operation Control | 0x YY00 0014 | D0: 0=Load, 1=Armed | RW |
| 6:Prom prog 1 | 0x YY00 0018 | D(31,0):status | R |
| 7:Prom prog 2 | 0x YY00 001C | D(7,0):TDI bitstream length | W |
| 8:Prom prog 3 | 0x YY00 0020 | D(31,0):prog bitstream in | W |
| 9:Prom prog 4 | 0x YY00 0024 | D(31,0):prog readback | R |

Daughter CSRs

| *ID: Name* | *Address* | *Functionality (default)* | *Access* |
|---|---|---|---|
| 0: Daughter firmware rev | 0x YY00 0100 | 0xDCBAmmnn (Major and Minor rev) | R |
| 1: Status | 0x YY00 0104 | 0xDAyymmdd - Date of this rev | R |
| 2: DSM Cables Connected | 0x YY00 0108 | D(7,0) | R |
| 3: Read/writable test reg | 0x YY00 010C | | RW |
| 4: FIFO Status | 0x YY00 0110 | D0: Token FIFO Empty<br>D1: Token FIFO Full<br>D2: Response FIFO Empty<br>D3: Response FIFO Full<br>D4: Info FIFO 1 Empty<br>D5: Info FIFO 1 Full<br>D6: Info FIFO 2 Empty<br>D7: Info FIFO 2 Full<br>D8: Info FIFO 3 Empty<br>D9: Info FIFO 3 Full<br>D10: Info FIFO 4 Empty<br>D11: Info FIFO 4 Full<br>D12: Info FIFO 5 Empty<br>D13: Info FIFO 5 Full<br>D14: Info FIFO 6 Empty<br>D15: Info FIFO 6 Full<br>D16: Info FIFO 7 Empty<br>D17: Info FIFO 7 Full<br>D18: Info FIFO 8 Empty<br>D19: Info FIFO 8 Full<br>D20: Info FIFO 9 Empty<br>D21: Info FIFO 9 Full<br>D22: Info FIFO 10 Empty<br>D23: Info FIFO 10 Full | R |

| | | | |
|---|---|---|---|
| 5: FIFO Reset | 0x YY00 0114 | D0: Clear Token FIFO<br>D1: Clear Response FIFOs<br>D2: Clear Info FIFOs | W |
| 6: Token FIFO | 0x YY00 0118 | D(11,0): Token | W |
| 7: Response FIFO 1 | 0x YY00 011c | D(23,0): Action Word | W |
| 8: Response FIFO 2 | 0x YY00 0120 | D(11,0): Token | W |
| 9: Info FIFO 1 | 0x YY00 0124 | D(15,0): AW Det Bitmask<br>D(19,16): AW DAQ Command<br>D(23,20): AW TRG Command | R |
| 10: Info FIFO 2 | 0x YY00 0128 | D(11,0): Token | R |
| 11: Info FIFO 3 | 0x YY00 012c | D(31,0): DSM tree bits (31,0) | R |
| 12: Info FIFO 4 | 0x YY00 0130 | D(31,0): DSM tree bits (63,32) | R |
| 13: Info FIFO 5 | 0x YY00 0134 | D(31,0): DSM tree bits (95,64) | R |
| 14: Info FIFO 6 | 0x YY00 0138 | D(31,0): DSM tree bits (127,96) | R |
| 15: Info FIFO 7 | 0x YY00 013c | D(31,0): Active triggers (31,0) | R |
| 16: Info FIFO 8 | 0x YY00 0140 | D(31,0): Active triggers (63,32) | R |
| 17: Info FIFO 9 | 0x YY00 0144 | D(15,0): External BUSY<br>D(32,16): Internal BUSY | R |
| 18: Info FIFO 10 | 0x YY00 0148 | D(15,0): DSM address | R |
| 19: Internal Busy | 0x YY00 014c | D(15,0): Enable per detector | RW |
| 20: Internal Busy Length | 0x YY00 0150 | D(31,0): in RS units | RW |
| 21: Local Address Control | 0x YY00 0154 | D0: Reset to zero<br>D1: Copy current value to CSR22<br>D2: Increment by one | W |
| 22: Read Local Address | 0x YY00 0158 | D(15,0): Address counter value | R |
| 23: TCD clock source | 0x YY00 015c | D0: 0=TCUI, 1=TCU | RW |
| 24: Snoop DSM inputs | 0x YY00 0160 | D(31,0): DSM tree bits (31,0) | R |
| 25: Snoop DSM inputs | 0x YY00 0164 | D(31,0): DSM tree bits (63,32) | R |
| 26: Snoop DSM inputs | 0x YY00 0168 | D(31,0): DSM tree bits (95,64) | R |
| 27: Snoop DSM inputs | 0x YY00 016c | D(31,0): DSM tree bits (127,96) | R |
| 28: Snoop Busy inputs | 0x YY00 0170 | D(15,0): External BUSY | R |
| 29: Token FIFO count | 0x YY00 0174 | D(11,0): Count | R |
| 30: INFO FIFO 1 count | 0x YY00 0178 | D(11,0): Count | R |
| 31: INFO FIFO 2 count | 0x YY00 017c | D(11,0): Count | R |
| 32: Output Data Delay | 0x YY00 0180 | D(2,0): Number of 66MHz ticks of output delay | RW |
| 33: 8xRHIC Clock Control | 0x YY00 0184 | D0: Reset 8xRHIC clock<br>D1: Reset 8xRHIC strobes | W |
| 34: 8xRHIC Clock Status | 0x YY00 0188 | D0: 1 = Locked on RHIC clock<br>0 = Not locked<br>D1,D2: Unused<br>D3: 0 = 8xRHIC clock toggling<br>1 = 8xRHIC clock stopped | R |

Trigger Registers
(for trigger xx)

| *ID: Name* | *Address* | *Functionality* | *Access* |
|---|---|---|---|
| 0: Condition 1, on | 0x YY10 xx00 | D(31,0): DSM bits (31,0) | RW |
| 1: Condition 1, on | 0x YY10 xx04 | D(31,0): DSM bits (63,32) | RW |
| 2: Condition 1, on | 0x YY10 xx08 | D(31,0): DSM bits (95,64) | RW |
| 3: Condition 1, on | 0x YY10 xx0c | D(31,0): DSM bits (127,96) | RW |
| 4: Condition 1, off | 0x YY10 xx10 | D(31,0): DSM bits (31,0) | RW |
| 5: Condition 1, off | 0x YY10 xx14 | D(31,0): DSM bits (63,32) | RW |
| 6: Condition 1, off | 0x YY10 xx18 | D(31,0): DSM bits (95,64) | RW |
| 7: Condition 1, off | 0x YY10 xx1c | D(31,0): DSM bits (127,96) | RW |
| 8:31: Not Implemented Yet | | | |
| 32: Detector on | 0x YY10 xx80 | D(15,0) | RW |
| 33: Detector off | 0x YY10 xx84 | D(15,0) | RW |
| 34: Prescale | 0x YY10 xx88 | D(31,0) | RW |
| 35: Prescale Counter Start | 0x YY10 xx8c | D(31,0) | RW |

| | | | |
|---|---|---|---|
| 36: Action Word | 0x YY10 xx90 | D(15,0): AW Det Bitmask<br>D(19,16): AW DAQ Command<br>D(23,20): AW TRG Command | RW |
| 37: Enable/Disable | 0x YY10 xx94 | D0: 0=Disable, 1=Enable | RW |
| 38: Prescale Fraction | 0x YY10 xx98 | D(6,0) | RW |
| 39: Prescale Fraction Start | 0x YY10 xx9c | D(6,0) | RW |

Counter Registers

| ID: Name | Address | Functionality | Access |
|---|---|---|---|
| 0: Daughter-2 firmware rev | 0x YY20 0000 | 0xFEDCmmnn (Major and Minor rev) | R |
| 1: Daughter-2 firmware date | 0x YY20 0004 | 0xDAyymmdd - Date of the rev | R |
| 2: Counter Control | 0x YY20 0008 | D0: Clear all counters<br>D1: Latch counter values<br>D2: Done reading | W |
| 3: Counter Status | 0x YY20 000c | D0: Data ready<br>D1: Error<br>D2: Overflow | R |
| 4: Reserved | 0x YY20 0010 | | |
| 5: Reserved | 0x YY20 0014 | | |
| 6: Reserved | 0x YY20 0018 | | |
| 7: Reserved | 0x YY20 001c | | |
| | | | |
| 8: U1:U2 Link Test 0 | 0x YY20 0020 | D(0-31): Test data from U1 | R |
| 9: U1:U2 Link Test 1 | 0x YY20 0024 | D(0-31): Test data from U1 | R |
| 10: U1:U2 Link Test 2 | 0x YY20 0028 | D(0-31): Test data from U1 | R |
| 11: U1:U2 Link Test 3 | 0x YY20 002c | D(0-31): Test data from U1 | R |
| 12: U1:U2 Link Test 4 | 0x YY20 0030 | D(0-31): Test data from U1 | R |
| 13: U1:U2 Link Test 5 | 0x YY20 0034 | D(0-31): Test data from U1 | R |
| 14: U1:U2 Link Test 6 | 0x YY20 0038 | D(0-31): Test data from U1 | R |
| 15: U1:U2 Link Test 7 | 0x YY20 003c | D(0-31): Test data from U1 | R |
| | | | |
| 16: Bunch Crossing (lo) | 0x YY20 0040 | D(0-31): Counter data 32 LSB | R |
| 17: Bunch Crossing (hi) | 0x YY20 0044 | D(0-7): Counter data 8 MSB | R |
| 18: TCU dead (lo) | 0x YY20 0048 | D(0-31): Counter data 32 LSB | R |
| 19: TCU dead (hi) | 0x YY20 004c | D(0-7): Counter data 8 MSB | R |
| 20: Triggers (lo) | 0x YY20 0050 | D(0-31): Counter data 32 LSB | R |
| 21: Triggers (hi) | 0x YY20 0054 | D(0-7): Counter data 8 MSB | R |
| 22: Responses (lo) | 0x YY20 0058 | D(0-31): Counter data 32 LSB | R |
| 23: Responses (hi) | 0x YY20 005c | D(0-7): Counter data 8 MSB | R |
| | 0x YY20 0060 - 0x YY20 00fc | Available space for extra registers | |
| | | | |
| For each Detector ZZ:<br>ZZ is in the range 0 to 15<br>For each ZZ there is a pair of registers<br>Register Address = 0xYY200100 + (ZZ<<3) + offset | | | |
| ZZ-0: Det-Live-ZZ (lo) | Offset = 0x0 | D(0-31): Counter data 32 LSB | R |
| ZZ-1: Det-Live-ZZ (hi) | Offset = 0x4 | D(0-7): Counter data 8 MSB | R |
| | | | |
| So, for example… | | | |
| ZZ=0 | | | |
| 0-0: Det-Live-0 (lo) | 0x YY20 0100 | D(0-31): Counter data 32 LSB | R |
| 0-1: Det-Live-0 (hi) | 0x YY20 0104 | D(0-7): Counter data 8 MSB | R |
| ZZ=1 | | | |
| 1-0: Det-Live-1 (lo) | 0x YY20 0108 | D(0-31): Counter data 32 LSB | R |
| 1-1: Det-Live-1 (hi) | 0x YY20 010c | D(0-7): Counter data 8 MSB | R |
| … and so on | | | |
| ZZ = 15 | | | |

| | | | |
|---|---|---|---|
| 15-0: Det-Live-15 (lo) | 0x YY20 0178 | D(0-31): Counter data 32 LSB | R |
| 15-1: Det-Live-15 (hi) | 0x YY20 017c | D(0-7): Counter data 8 MSB | R |
| | | | |
| | 0x YY20 0180 - 0x YY20 01fc | Available space for extra pairs of detector-live registers | |
| | | | |
| For each Trigger XX:<br>XX is in the range 0 to 31<br>For each XX there is a group of 8 registers<br>Register Address = 0xYY210000 + (XX<<5) + offset | | | |
| XX-0: PHYS-XX (lo) | Offset = 0x0 | D(0-31): Counter data 32 LSB | R |
| XX-1: PHYS-XX (hi) | Offset = 0x4 | D(0-7): Counter data 8 MSB | R |
| XX-2: PHYS+LIVE-XX (lo) | Offset = 0x8 | D(0-31): Counter data 32 LSB | R |
| XX-3: PHYS+LIVE-XX (hi) | Offset = 0xc | D(0-7): Counter data 8 MSB | R |
| XX-4: PHYS+LIVE+PS-XX (lo) | Offset = 0x10 | D(0-31): Counter data 32 LSB | R |
| XX-5: PHYS+LIVE+PS-XX (hi) | Offset = 0x14 | D(0-7): Counter data 8 MSB | R |
| XX-6: Spare-XX (lo) | Offset = 0x18 | D(0-31): Counter data 32 LSB | R |
| XX-7: Spare-XX (hi) | Offset = 0x1c | D(0-7): Counter data 8 MSB | R |
| | | | |
| So, for example… | | | |
| XX = 0 | | | |
| 0-0: PHYS-0 (lo) | 0x YY21 0000 | D(0-31): Counter data 32 LSB | R |
| 0-1: PHYS-0 (hi) | 0x YY21 0004 | D(0-7): Counter data 8 MSB | R |
| 0-2: PHYS+LIVE-0 (lo) | 0x YY21 0008 | D(0-31): Counter data 32 LSB | R |
| 0-3: PHYS+LIVE-0 (hi) | 0x YY21 000c | D(0-7): Counter data 8 MSB | R |
| 0-4: PHYS+LIVE+PS-0 (lo) | 0x YY21 0010 | D(0-31): Counter data 32 LSB | R |
| 0-5: PHYS+LIVE+PS-0 (hi) | 0x YY21 0014 | D(0-7): Counter data 8 MSB | R |
| 0-6: Spare-0 (lo) | 0x YY21 0018 | D(0-31): Counter data 32 LSB | R |
| 0-7: Spare-0 (hi) | 0x YY21 001c | D(0-7): Counter data 8 MSB | R |
| XX = 1 | | | |
| 1-0: PHYS-1 (lo) | 0x YY21 0020 | D(0-31): Counter data 32 LSB | R |
| 1-1: PHYS-1 (hi) | 0x YY21 0024 | D(0-7): Counter data 8 MSB | R |
| 1-2: PHYS+LIVE-1 (lo) | 0x YY21 0028 | D(0-31): Counter data 32 LSB | R |
| 1-3: PHYS+LIVE-1 (hi) | 0x YY21 002c | D(0-7): Counter data 8 MSB | R |
| 1-4: PHYS+LIVE+PS-1 (lo) | 0x YY21 0030 | D(0-31): Counter data 32 LSB | R |
| 1-5: PHYS+LIVE+PS-1 (hi) | 0x YY21 0034 | D(0-7): Counter data 8 MSB | R |
| 1-6: Spare-1 (lo) | 0x YY21 0038 | D(0-31): Counter data 32 LSB | R |
| 1-7: Spare-1 (hi) | 0x YY21 003c | D(0-7): Counter data 8 MSB | R |
| … and so on | | | |
| XX = 31 | | | |
| 31-0: PHYS-31 (lo) | 0x YY21 03e0 | D(0-31): Counter data 32 LSB | R |
| 31-1: PHYS-31 (hi) | 0x YY21 03e4 | D(0-7): Counter data 8 MSB | R |
| 31-2: PHYS+LIVE-31 (lo) | 0x YY21 03e8 | D(0-31): Counter data 32 LSB | R |
| 31-3: PHYS+LIVE-31 (hi) | 0x YY21 03ec | D(0-7): Counter data 8 MSB | R |
| 31-4: PHYS+LIVE+PS-31 (lo) | 0x YY21 03f0 | D(0-31): Counter data 32 LSB | R |
| 31-5: PHYS+LIVE+PS-31 (hi) | 0x YY21 03f4 | D(0-7): Counter data 8 MSB | R |
| 31-6: Spare-31 (lo) | 0x YY21 03f8 | D(0-31): Counter data 32 LSB | R |
| 31-7: Spare-31 (hi) | 0x YY21 03fc | D(0-7): Counter data 8 MSB | R |