

Special Trigger Algorithm
11_st201_2010_c.rbt

January 7, 2010

Change Log:

Version	Date	Comment
2010_a	December 7, 2009	First version for 2010. Removed the old special trigger logic and replaced it with the new laser logic.
2010_b	January 6, 2010	Moved the laser_fire output bit from bit 1 to bit 13 in the output list.
2010_c	January 7, 2010	Moved the laser_fire bit back to its original location. Moved the input bits from bits 0 and 1 of channel 0 to bits 4 and 5. Also added a copy of the unmodified input bits to the output list.

Input Bits

Input Channel	Bit Description
0	Bits 0:3 – Unused Bit 4 – Laser lamp Bit 5 – Laser diode Bits 6:15 – unused
1:7	Unused

Registers

Register	Register Description
0	16 LSB of 32-bit Zero-Bias prescale
1	16 MSB of 32-bit Zero-Bias prescale
2	12 LSB of 24-bit random bit generator rate
3	12 MSB of 24-bit random bit generator rate
4	16-bit Laser protection length
5:12	Unused
13	1-bit command to latch current value of clock counters
14	12 LSB of 24-bit clock counter
15	12 MSB of 24-bit clock counter

Output Bits

Bit	Name	Description
Bit 0	Laser-protection	Laser is about to fire so no physics triggers should be issued
Bit 1	Laser-fire	Laser firing
Bit 2	Laser-lamp	Copy of the original Laser lamp input signal
Bit 3	Laser-diode	Copy of the original Laser diode input signal
Bits 4:13	N/A	Unused
Bit 14	Zero-bias	Zero-bias
Bit 15	Random	Random
Bits 16:31		Same as bits 0:15

Internal Logic

- The incoming laser lamp and diode signals are copied to the output, unmodified but with the appropriate delay.
- When the laser lamp signal turns on, the laser protection output is generated for the number of RHIC clock ticks specified in register 4.
- When the laser diode signal turns on, the laser firing output is set for just one tick of the RHIC clock.
- When the DSM is put into RUN mode the 24-bit clock counter starts from 0 and increments by 1 every tick of the RHIC clock.
- When the user writes to register 13 the current value of the clock counter is copied into registers 14 (the 12 LSB) and 15 (the 12 MSB) which can then be read out by the user.
- If a non-zero value is set for the zero-bias prescale (Reg. 0 and 1) then a counter starts from the prescale value and decrements by 1 every tick of the RHIC clock. When the current value of the counter reaches 1 the zero-bias bit is set, and the counter is reset to the starting value specified in the prescale registers.
- If a non-zero value is set in the random generator registers (Reg. 2 and 3) then the random bit generator is started. The register values are used to set the rate of exponential decay of a 32-bit number. When this number drops below a threshold value, chosen from a 128-bit linear feedback shift register, the random output bit is set. At this point the decaying number is reset to its maximum (all bits high) and a new threshold value is chosen from the shift register.